VLSI Circuit Design using Cadence EDA tools

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INFORNATION

- **Schedule: 20-21 Feb, 2017.**
- **Venue: ECAD Lab, 1st floor.**
- **Audience: Faculty ECE/CCE. Staff ECE/CCE, UG-PG Students.**

AGENDA

Day 1: 20/02/2017
Session 1: 2:00 PM to 5:00 PM.
Topics to be covered:

- Analog Design- MOSFET characterization.
- Inverter - The Circuit Perspective.
- Schematic Capture and Simulation.
- CMOS Inverter Design and Characterization: VTC, DC Static Performance, Delay Characterization, Power Dissipation.
- Backgrounder for PDK, Inverter, Standard Cells, Designing, Transistor Switch Models.
- Hand-holding on the Layout of Inverter.
- CMOS Fabrication Technology Review and Background for Layout Design Rules.
- Setting up Post Layout Simulation environment and simulate.
- Noise Margin concept /calculate NM of designed Inverter.
- Inverter as Amplifier.

Day 2: 21/02/2017
Session 2: 9:00 AM to 1:00 PM.
Session 3: 2:00 PM to 5:00 PM.
Topics to be covered:

- ASIC/Digital Design- Up-Down Counter (8bit).
- RTL coding and Functional simulation.
- Synthesis gate level netlist/Post synthesis Simulation/Timing Simulation, power,area and timing information.
- Floor-planning, power planning, placement.
- CTS, Automatic Routing.
- Timing Debugging - Setup and Hold violation.
- Timing slack/Max Operating frequency.
- XRC and Post layout simulation.
- GDSII.